

[THE USE OF A LAYOUT-OPTIMIZATION TOOL TO INCREASE THE YIELD AND RELIABILITY OF VLSI DESIGNS]

Abstract

The invention provides a method and structure for optimizing placement of redundant vias within an integrated circuit design. The invention first locates target vias by determining which vias do not have a redundant via. Then, the invention draws marker shapes on or adjacent to the target vias. The marker shapes are only drawn in a horizontal or vertical direction from each of the target vias. Next, the invention simultaneously expands all of the marker shapes in the first direction to a predetermined length or until the marker shapes reach the limits of a ground rule. During the expanding, different marker shapes will be expanded to different lengths. The invention determines which of the marker shapes were expanded sufficiently to form a valid redundant via to produce a first set of potential redundant vias and the invention eliminates marker shapes that could not be expanded sufficiently to form a valid redundant via. The invention repeats the foregoing processing in the direction perpendicular to the first. The inven-

tion can also be used to eliminate certain undesirable structures such as stacked vias or can be used to fix other problems such as insufficient via-to-via spacing. The invention then adds the redundant vias to the integrated circuit design, according to output produced by the optimizer.